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JAPANESE JOURNAL OF APPLIED PHYSICS, Supplements, 16th Int. Conf. Solid State Devices and Materials, Tokyo, 30th September - 1st October 1984, pages 265-268, Tokyo, JP; H.SHICHIJO et al.: "TITE RAM : a new SOI DRAM gain cell for Mbit DRAM's"

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transistor, the drain of the read select transistor being the drain of the dual gate transistor and the source of the storage transistor being the source of the dual gate transistor, between which drain and source the channel region of the dual gate transistor lies, and the two gates of the dual gate transistor being, respectively, the gate of the read select transistor and the gate of the storage transistor, which gates overlie the channel region of the dual gate transistor via an interposed insulator layer,

and characterised in that

the write select transistor is formed over the read select transistor, with an interposed insulator layer, the drain of the write select transistor being connected directly to the drain of the read select transistor through a window or opening in the latter interposed insulator layer,

and in that

the source region of the write select transistor acts also as the gate of the storage transistor which is otherwise provided on the same side of the latter interposed insulator layer as the read select transistor.

An embodiment of the present invention can provide a three-transistor cell for a DRAM having a structure enabling a higher packaging density to be achieved for the DRAM device.

An embodiment of the present invention can provide a three-transistor cell for a DRAM with a two-storied structure wherein an arrangement of elements and associated control lines of the cell is provided which is effective to reduce the area of the cell.

An embodiment of the present invention can provide a configuration for a three-transistor cell of a DRAM device which enables a reduction of the number of control lines from three to two (not including a ground line).

An embodiment of the present invention provides a structure for a cell of a DRAM device wherein electrical elements are arranged in a two-storied configuration such that a high packing density can be realized.

Embodiments of the present invention provide such two-storied structures of three transistor cells of DRAMS whereby the cells have either three or two driving lines besides a ground line.

In the above description of the previously proposed three-transistor memory cell shown in Fig. 1, it should be noted that transistor T_1 and transistor T_3 are both conductive when reading a stored signal "O", passing a current through the T_1-T_3 circuit between data bit line DL and ground line GND, but that transistor T_1 is conductive and transistor T_3 is non-conductive when a stored signal "1" is read and in this case no current flows through the T_1-T_3 circuit.

The inventor has appreciated that a dual gate field effect transistor can be applied in the cell of Fig. 1, by which the connection between transistor T_1 and transistor T_3 through respective source-drain regions can be omitted, serving to effect an economy as regards space on the relevant substrate of a DRAM device. This is applied in (some) embodiments of the present invention.

For saving area on a substrate of a semiconductor device, two-storied or two-level structures have been utilized, wherein electronic elements are arranged in two layers separated from one another by an insulator layer.

In an embodiment of the present invention, a read select transistor T_1, a storage transistor T_3, and a read select line RL which acts as a gate electrode of transistor T_1 are formed directly on the surface of a silicon substrate, i.e. on a first storey or level, whilst a write select transistor T_2 and a write (word) select line WL which acts as a gate of transistor T_2 are formed on a second storey, on an insulator layer separating the first and second stories. A data bit line DL is formed on a phosphosilicate glass layer covering the entire substrate.

In a DRAM memory cell in accordance with an embodiment of the present invention, the arrangement of the transistors is such that the write select transistor T_2 overlies the read select transistor T_1, and a common channel region is formed partially overlaid by the gates of read select transistor T_1 and storage transistor T_3. Thus the transistors T_1 and T_3 act like a dual gate transistor. As a result, in respect of the connecting portion between the two transistors, usually including at least source-drain regions, a remarkable saving is made. In addition, due to the overlying structure of transistor T_2 on transistor T_1 and the circuit configuration of the cell, one of the source-drain regions of transistor T_2 is utilized also as the gate electrode of transistor T_3, serving to save space on the substrate.

Furthermore, in accordance with an embodiment of the present invention, a circuit configuration of a DRAM cell is provided wherein the number of control lines of a memory cell is reduced from three to two; namely, a shared write/read bit line and a shared write/read select line, and two cell transistors having different threshold voltages from each other are used. A DRAM cell having a further simplified two-storied structure is provided in accordance with the circuit configuration of the cell.

Reference is made, by way of example, to the accompanying drawings, in which:-

Fig. 1 is a schematic circuit diagram of a previously proposed three transistor DRAM cell;

Fig. 2 (a) is a schematic circuit diagram of a three-transistor DRAM cell in accordance with a first embodiment of the present invention;

Fig. 2 (b) is a partial plan view illustrating the

pendicular to the Y-direction, being connected to the drain regions 9a and 3a through a contact hole 13b (Fig. 2 (c), see also 13 in Fig. 2 (b)) opened in the phosphosilicate glass layer 12. The source region 3b is extended to serve as a ground line GND as shown in the plan view of Fig. 2 (b). Thus the circuit configuration shown in Fig. 2 (a) is realized.

To write a logical "O" into the cell, the data bit line DL is maintained at a high level and the write select line WL, namely the gate electrode 11 of the write select transistor T_2, is brought to a higher voltage level to make the write select transistor T_2 "ON", bringing the gate electrode 9b of the storage transistor T_3 to high level to keep the transistor T_3 in "ON" state. Thereafter, the write select transistor T_2 is made "OFF" to keep the voltage level of the gate electrode 9b of the storage transistor T_3 high, storing the logical "O".

When reading a stored logical "O" from the cell, the data bit line DL is brought to a predetermined voltage level such as an intermediate voltage Vm level between high level and low level and kept floating. Thereafter, the read select transistor T_1 is made "ON". Since the storage transistor T_3 is in an "ON" state, a current flows from the data bit line DL to the ground line GND through the read select transistor T_1 and the storage transistor T_3 substantially pulling down the voltage of the data bit line DL to the ground voltage. The reduction of the voltage of the data bit line DL represents the logical "O".

For writing a logical "I" into the cell, the data bit line DL is maintained at a low voltage level, and simultaneously the write select transistor T_2 is made "ON", making the voltage level of the gate of the storage transistor T_3 low. Then, the write select transistor T_2 is made "OFF" thereafter, maintaining the gate voltage level of the storage transistor T_3 low, namely, maintaining the storage transistor T_3 in "OFF" state.

When reading out the logical "I" from the cell, the data bit line DL is maintained at the voltage level Vm, for instance, and the read select transistor T_1 is made "ON". Since the storage transistor T_3 is "OFF" state, no current flows through the circuit storage transistor T_3 plus read select transistor T_1, maintaining the voltage of the data bit line DL at Vm, providing no voltage difference (no pull-down of the data bit line voltage) which represents the logical "1".

As described above, the circuitry of the first embodiment of the present invention operates in the same manner as that of a previously prepared DRAM cell. However, the storage transistor T_3 and the read select transistor T_1 co-possess their channel regions Ch3 and Ch1, eliminating diffusion regions for connecting the two transistors. Furthermore, one of the source-drain regions of the write select transistor T_2 is commonly used as the gate electrode of the storage transistor T_3. As the result, a remarkable reduction in cell area can be achieved, enabling packing density to be increased significantly.

In addition, the gate electrode 9b of the storage transistor T_3 wherein information is stored in the form of electrical charges, is electrically isolated from the substrate 1 by the surrounding silicon dioxide layer 6 and 7, resulting in an effect which serves for preventing soft error problems, due to alpha ray irradiation.

The circuit configuration of Fig. 2 (a) can be illustrated in another configuration as shown in Fig. 2 (d), wherein the read select transistor T_1 and the storage transistor T_3 are replaced by a dual-gate electrode MOS transistor T_d. It will be apparent from the above description of the first embodiment of the present invention, for those skilled in the art, that both circuit configurations are entirely the same with regard to circuit operation.

Now, a second embodiment in accordance with the present invention will be described with reference to Figs. 3 (a) to 3 (c). The memory cell of the second embodiment has three transistors and two control lines as shown in the circuit diagram of Fig. 3 (a). In comparison with the cell of Fig. 2 (a), the read select line RL and write select line WL of Fig. 2 (a) are replaced by a single line, write/read select line WRL to which the gate electrodes of a write select transistor T_2 and read select transistor T_1 are connected. Therefore, in order to distinguish these two transistors from each other, the threshold voltages of the two transistors T_1 and T_2, namely V_{th1} and V_{th2} respectively, are made different from each other. Thus control lines are reduced by one, and the resulting cell structure is further simplified.

Fig. 3 (b) is a partial plan view of a DRAM device, illustrating the configuration of a memory cell in accordance with the second embodiment, and Fig. 3 (c) is a cross-sectional view of the cell taken along the line A-A shown in the partial plan view of Fig. 3 (b).

Threshold voltages of transistors T_1, T_2 and T_3 are designated by V_{th1}, V_{th2} and V_{th3} respectively, and voltage levels of write/read select line WRL for selecting a reading or a writing operation are designated by V_r and V_w respectively. The voltage level of the data bit line DL, namely a data signal is designated by V_d.

Taking the threshold voltage of storage transistor T_3 as $V_{th3}=V_{th1}$, the relationships required for the above threshold voltage levels are as follows:

$V_{th1} < V_r < V_{th2}$ (read out condition)
$V_d + V_{th2} < V_w$ (write in condition)
$V_{th1} < V_d$ (readable condition).

the SOI (silicon on insulator) technologies and the single crystal silicon layer is referred to as an SOI layer 8 which serves to form an MOS FET having a small gate leakage current. At the next step, the SOI layer 8 is doped, to become a p-type diffusion layer with 10^{15} cm^{-3} dopant density, by boron (B+) ion implantation and subsequent heat treatment.

There is an alternative method for forming the SOI layer 8 utilizing an SOI technology, namely solid phase epitaxy. A polycrystalline silicon layer formed on the entire substrate by a conventional CVD method may be converted into a layer of single crystal silicon structure by re-crystallization using a heat treatment at approximately 600 °C whereby the exposed single crystal structure of the contact region acts as seed for the recrystallization.

Referring to Fig. 5 (c):-

Subsequently, the SOI layer 8 and the second gate insulator layer 7 are patterned simultaneously to expose a source region including a ground region, a third gate insulator region 10 approximately 300 Å thick is formed by a thermal oxidizing method. This step is followed by a chemical vapour deposition (CVD) process to form a tungsten silicide (WSi_2) layer of approximately 2000 Å thickness, accompanied by a photolithographic process for patterning a gate electrode 11 of a write select transistor T_2. The gate electrode 11 is extended to play a rôle as a word select line WL.

Referring to Fig. 5 (d):-

The next step is ion implantation of arsenic ions (As+) with approximately $5X10^{15}$ dose and with an accelerating energy of approximately 120 KeV over the entire substrate, followed by a predetermined heat treatment, forming a first n+ type region 9a as a drain region of write select transistor T_2, a second n+ region 9b as a source region of write select transistor T_2, and an n+ type source region 3b. The source region 3b of storage transistor T_3 is extended to act as a ground line. The above-described n+ type regions 9a and 9b are formed to reach the underlying SOI layer 8.

Referring to Fig. 5 (e):-

The entire substrate is then covered with a phosphosilicate glass layer 12 by a conventional method, and a contact window 13b is formed to expose the underlying drain region 3a of read select transistor T_1. Subsequently, by a conventional method, a data bit line DL of aluminium or other metal is formed over the phosphosilicate glass layer 12 so that the data bit line DL is connected to the drain region 9a of write select transistor T_2 and the drain region 3a of read select transistor T_1 through the contact window 13b. Finally, formation of a passivating layer for the substrate and other final processes (not shown) are performed to complete the semiconductor memory device.

As described above in detail, through all the fabricating steps of the semiconductor memory device, conventional semiconductor fabricating technologies are used, requiring no increase in the fabrication cost.

A dynamic random access memory (DRAM) cell having three MIS transistors arranged in two-storied layers having a high packing density configuration is disclosed. A write select transistor is disposed overlying a read select transistor, being electrically separated from each other through an insulator layer, and a drain region of the write select transistor is shared with the underlying read select transistor as its gate electrode. A storage transistor and the read select transistor are formed on a silicon substrate in the same level and channel regions of both transistors are connected to each other and used as a diffusion region of the opposite transistor, resulting in elimination of connecting members such as diffusion regions and a conducting path therebetween which were otherwise necessary. These two points contribute to elevate the packing density of the cell. Furthermore, a write select line and a read select line are combined into a single control line: write/read select line, saving one line to obtain higher packing density. In the cell, gate electrodes of both transistors are connected to the write/read line. These transistors are distinguished from each other by their different threshold voltage levels from each other.

Claims

1. A three-transistor cell for a dynamic random access memory formed on a semiconductor substrate (1), the cell comprising

a read select transistor (T_1), having a drain (3a) connected to a data bit line (DL) of the memory, and a gate (5, 15) connected to a read select line (RL, WRL) of the memory,

a storage transistor (T_3), having a drain (Ch1) connected to a source (Ch3) of the read select transistor (T_1) and a source (3b) connected to a ground line (GND) of the memory, and

a write select transistor (T_2) having a source (9b) connected to a gate (9b) of the storage transistor, a gate (11, 15) connected to a write select line (WL, WRL) of the memory, and a drain (9a) connected to the data bit line (DL),

characterised in that

the read select transistor (T_1) and the storage transistor (T_3) are formed as a dual gate transistor (T_1, T_3; T_d), a channel region (Ch1) of the read select transistor being directly con-

source du transistor à double grille, la région de canal (Ch1, Ch3) du transistor à double grille étant placée entre le drain (3a) et la source (3b) et les deux grilles du transistor à double grille étant respectivement la grille (5, 15) du transistor de sélection de lecture et la grille (9b) du transistor de stockage, ces grilles reposant sur la région de canal (Ch1, Ch3) du transistor à double grille via une couche isolante interposée (4, 7),
et caractérisée en ce que :

le transistor de sélection d'écriture (T_2) est formé sur le transistor de sélection de lecture (T_1) avec une couche isolante interposée (6, 7 ; 6, 7, 10), le drain (9a) du transistor de sélection d'écriture étant directement connecté au drain (3a) du transistor de sélection de lecture au travers d'une fenêtre ou ouverture ménagée dans la seconde couche isolante interposée,
et en ce que :

la région de source (9b) du transistor de sélection d'écriture (T_2) se comporte également comme la grille du transistor de stockage (T_3) qui est sinon prévue sur le même côté de la seconde couche isolante interposée que le transistor de sélection de lecture.

2. Cellule selon la revendication 1, dans laquelle le transistor de sélection de lecture (T_1) et le transistor de sélection d'écriture (T_2) partagent une grille commune (15) qui est connectée à une ligne de sélection de lecture/écriture combinées (WRL) de la mémoire, le transistor de sélection de lecture et le transistor de sélection d'écriture ayant des couches isolantes de grille respectives (4, 10) et des tensions de seuil respectives différentes (Vth1, Vth2).

3. Cellule selon la revendication 2, dans laquelle ledit transistor de sélection de lecture (T_1) et ledit transistor de sélection d'écriture (T_2) qui est formé au-dessus dudit transistor de sélection de lecture (T_1) partagent une électrode de grille commune (15-figure 3(c)) l'un avec l'autre, ladite électrode de grille commune (15) étant placée entre ledit transistor de sélection de lecture (T_1) et ledit transistor de sélection d'écriture (T_2) et étant efficace pour les transistors respectifs au travers des couches isolantes de grille respectives (4, 10).

4. Cellule selon la revendication 1, dans laquelle ledit transistor de stockage (T_3) comporte une électrode de grille, des parois latérales de celle-ci étant recouvertes par des couches isolantes.

5. Cellule selon la revendication 2, dans laquelle les parois latérales de ladite électrode de grille commune (15) sont recouvertes par des couches isolantes.

6. Cellule selon la revendication 1, dans laquelle ledit transistor de sélection d'écriture (T_2) est formé dans une couche semiconductrice (8) formée sur une couche isolante interposée (7) au-dessus dudit transistor de sélection de lecture (T_1), cette couche semiconductrice étant par exemple une couche en silicium monocristallin fabriquée en utilisant une technologie silicium-sur-isolant (SOI).

Patentansprüche

1. Drei-Transistor-Zelle für einen dynamischen Speicher mit wahlfreiem Zugriff, der auf einem Halbleitersubstrat (1) gebildet ist, welche Zelle umfaßt,

einen Leseauswahltransistor (T_1), der ein Drain (3a) hat, das mit einer Datenbitleitung (DL) des Speichers verbunden ist, und ein Gate (5, 15), das mit einer Leseauswahlleitung (RL, WRL) des Speichers verbunden ist,

einen Speichertransistor (T_3), der ein Drain (Ch1) hat, das mit einer Source (Ch3) des Leseauswahltransistors (T1) verbunden ist, und eine Source (3b), die mit einer Erdleitung (GND) des Speichers verbunden ist, und

einem Schreibauswahltransistor (T_2), der eine Source (9b) hat, die mit einem Gate (9b) des Speichertransistors verbunden ist, ein Gate (11, 15), das mit einer Schreibauswahlleitung (WL, WRL) des Speichers verbunden ist, und ein Drain (9a), das mit der Datenbitleitung (DL) verbunden ist,

dadurch gekennzeichnet, daß

der Leseauswahltransistor (T_1) und der Speichertransistor (T_3) als ein Dual-Gate-Transistor (T_1, T_3; T_d) gebildet sind, ein Kanalbereich (Ch1) des Leseauswahltransistors direkt mit einem Kanalbereich (Ch3) des Speichertransistors verbunden ist, um einen Kanalbereich (Ch2, Ch3) des Dual-Gate-Transistors zu bilden, der Kanalbereich (Ch1) des Leseauswahltransistors auch als Drain des Speichertransistors wirkt und der Kanalbereich (Ch3) des Speichertransistors auch als Source des Leseauswahltransistors wirkt, das Drain (3a) des Leseauswahltransistors ein Drain des Dual-Gate-Transistors ist, und die Source (3b) des Speichertransistors die Source des Dual-Gate-Transistors ist, zwischen welchem Drain (3a) und Source (3b) des Kanalbereichs (Ch1,Ch3) des Dual-Gate-Transistors liegt, und die beiden Gates des Dual-Gate-Transistors jeweils das Gate (5, 15) des Leseauswahltransistors bzw.

FIG. 1

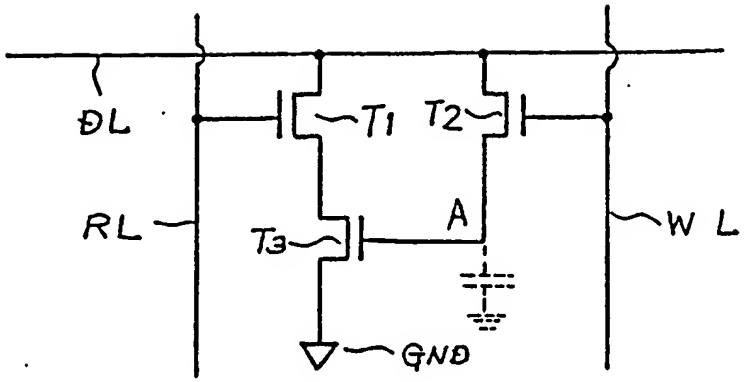

FIG. 2(d)

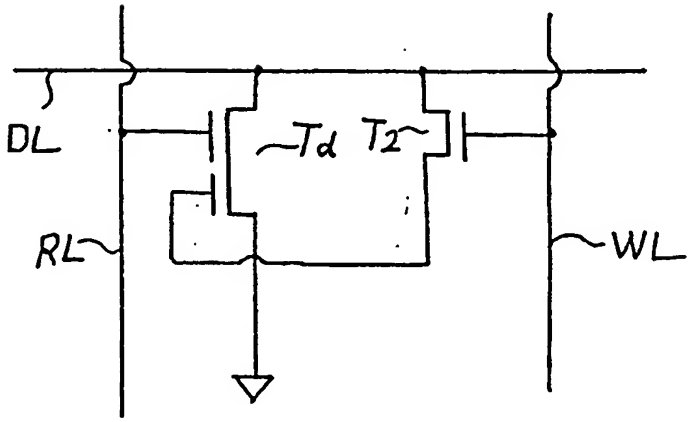

FIG.3(a)

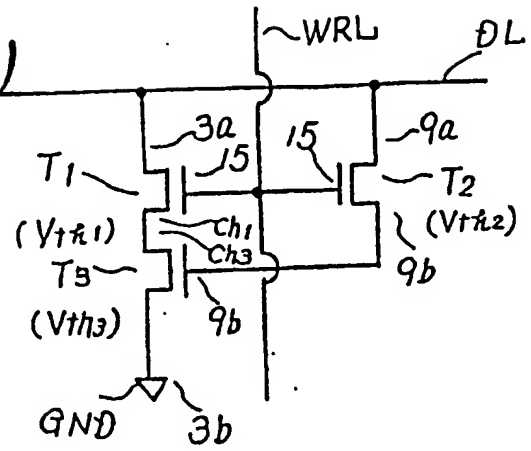

FIG.3(b)

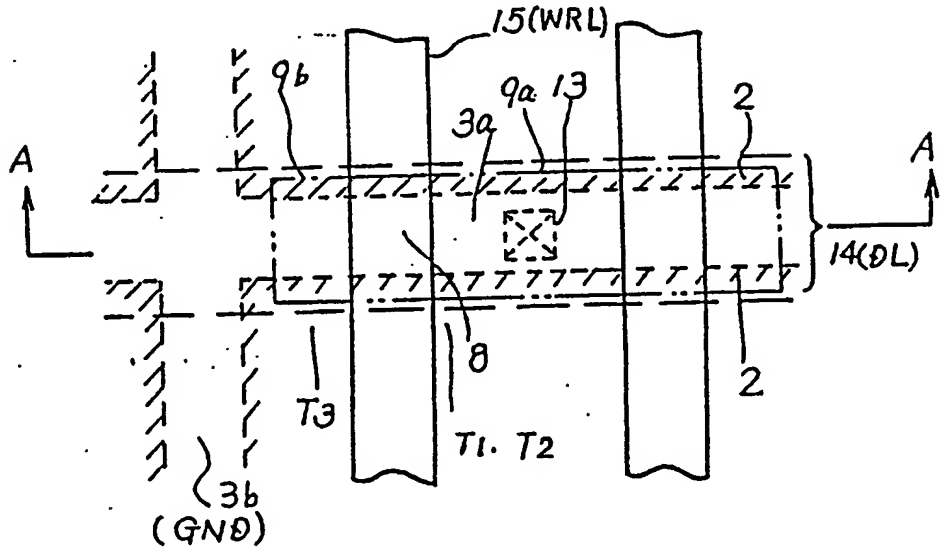

FIG.3(c)

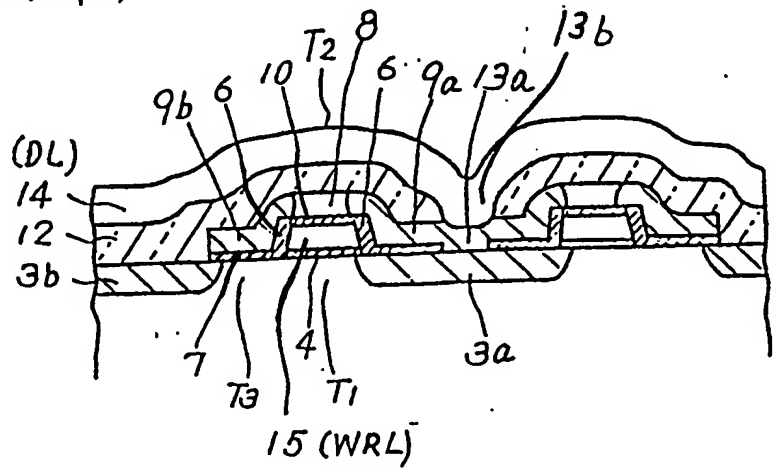

FIG. 5(c)

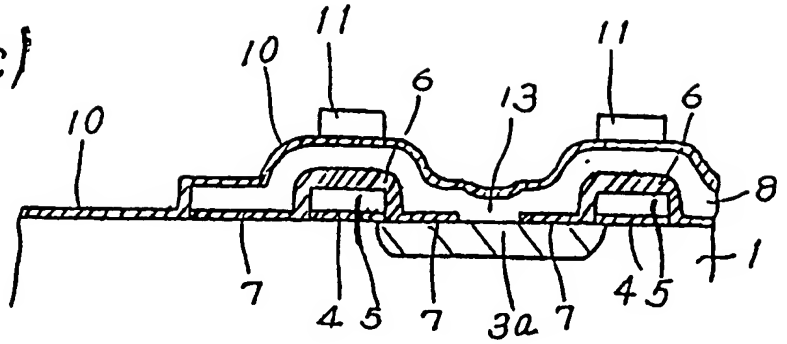

FIG. 5(d)

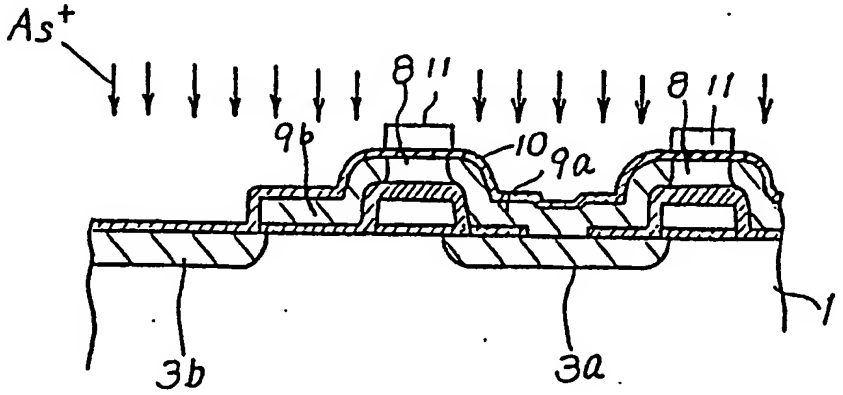

FIG. 5(e)